REMARKS

Claims 1-17 are pending in the application. The status of these claims is as follows:

Claims / Section	35 U.S.C. Sec.	References / Notes
4, 6, 7, 11 & 13	Objection	• Dependent upon a rejected base claim, but otherwise allowable.
1, 3, 5, 8-10, 12 & 14-15	§103(a) Obviousness	• Admitted Prior Art; and • Tanaka (U.S. Patent No. 5,513,178).
16, 17	§103(a) Obviousness	• Admitted Prior Art; • Tanaka (U.S. Patent No. 5,513,178); and • Kobayashi, et al. (U.S. Patent No. 5,566,179).

Applicant thanks the Examiner for indicating the allowability of claims 4, 6, 7, 11 and 13, and provides discussion below for distinguishing the present invention from the art cited against it.

35 U.S.C. §103(a), CLAIMS1, 3, 5, 8-10, 12 & 14-17 OBVIOUSNESS OVER APA IN VIEW OF TANAKA

The present invention is non-obvious in view of APA and Tanaka because, although a receiver-side serial-parallel conversion generally described in Tanaka, Tanaka does not disclose the detailed steps of converting the digital data into units that respectively comprise and identical plurality of bits from each of said data channels, or of successfully dividing, beginning with said first data unit of said cell corresponding to said characteristic bit sequence, individual bits of each said data unit of said corresponding cell onto a plurality of data channels

of an output side of said receiver corresponding in number to said plurality of data channels of said input side.

The application subject matter is directed to a method and an ATM transfer system to transfer data in which digital data transmitted via parallel data channels are converted in a transmitter from parallel to serial, whereby the data transferred at the transmitter in parallel via a plurality of data channels are inserted into data units comprising a specific number of bits per data channel.

A specific number of data units are thus respectively combined into a cell and subsequently transferred serially to the receiver, where the cells are comprised of an external cell header comprising a characteristic bit sequence and an information portion comprising the useable data. However, the characteristic sequence can be inserted both into the external cell header and into an internal cell header. The additional internal cell header is added to the ATM cell already comprising an external cell header for the routing of the cell within the ATM transfer system.

The characteristic bit sequence arranged in an internal cell header is provided in asynchronously operating transfer systems realized until now for internal synchronization of the transmitter and the receiver. Internal switching information – among other things also the characteristic bit sequence – that are generated via a previously implemented evaluation of the address or control information provided in the external cell header are entered into the internal cell header. Thus, for example, path information necessary for the further routing of

the ATM cell expanded by the internal cell header are read out exclusively from the internal cell header into the coupler fields of an ATM transmission device.

The path information in the internal cell header is thereby represented with a lower number of bits in comparison with the path information provided in the external cell header, whereby a fast evaluation of the path information in the coupler device is enabled with the aid of a fast hardware logic. This is particularly necessary for the realization of the high data throughput rates required for ATM broadband communication networks.

Furthermore, the cells transmitted serially and respectively comprising the characteristic bit sequence in the internal or external cell header are received in a receiver, and the received cell stream is monitored upon the occurrence of the characteristic bit sequence arranged within the internal or external cell header for the purpose of being able to determine the first data unit of the corresponding cells in an advantageous manner after establishing the characteristic bit sequence in the receiver with the aid of the characteristic bit sequence.

Beginning with the previously determined first data unit, the individual bits of each data unit of the respective cell are separated into a specific number of data channels arranged in parallel. Finally, a parallel output of the bits of each data unit ensues via the corresponding output-side data channels arranged in parallel.

The inventive method serves in particular for realization of a receiver-side demultiplexing, meaning a serial-parallel conversion without significant circuit expenditure and without addition of additional synchronization information,

especially the addition of synchronization information that increases the number of the redundant information transferred with the aid of the transfer system, and thus reducing the transfer capacities available for the transfer of useful information. A receiver-side serial-parallel conversion is namely mentioned in Tanaka in general form, however it is in no way explicitly explained in which manner the mentioned serial-parallel conversion is implemented. Tanaka addresses the use of buffering for the temporary storage of incoming cells (see 6/15-16) and operates to recognize and predict congestion (6/17-19). The use of buffering and congestion avoidance of Tanaka does not server to operate in the same manner as the present invention—the focus of the present invention is not in dealing with congestion, but rather to make the receiver demultiplexing efficient, without additional costs or requiring additional synchronization information.

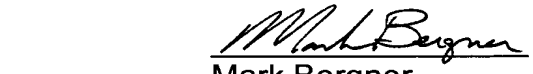
As a result, it is to be determined that an effective serial-parallel conversion or, respectively, demultiplexing can be realized with the aid of the inventive method and the ATM transfer system in the receiver of an ATM transfer system without the additional of additional redundancy in the serial cell stream. Thus a lesser circuit expenditure is necessary for the transmission of digital multiplexed data according to the ATM transfer principle. Furthermore, the use of the invention method enables the use of smaller module sizes for the transmitter or, respectively, receiver components within the ATM transfer system, which leads to a reduction of costs.

For these reasons, Applicant asserts that the language of the independent claims in the patent application are not obvious over APA in view of Tanaka (or, in combination with Kobayashi, cited by the Examiner as obviating elements of other dependent claims and not the independent claims), and respectfully request that the Examiner withdraw the §103(a) rejection from the present application.

CONCLUSION

Inasmuch as each of the objections have been overcome by the arguments presented above, and all of the Examiner's suggestions and requirements have been satisfied, it is respectfully requested that the present application be reconsidered, the rejections be withdrawn and that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

 (Reg. No. 45,877)

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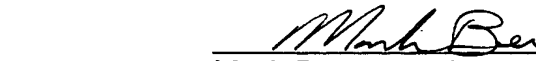

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